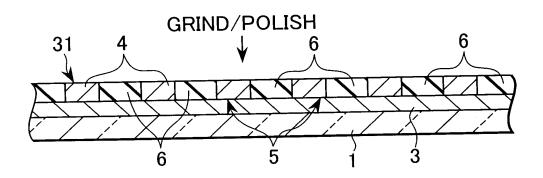
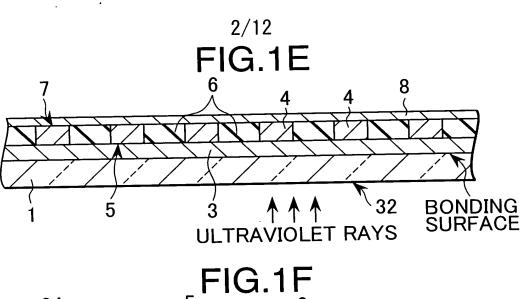
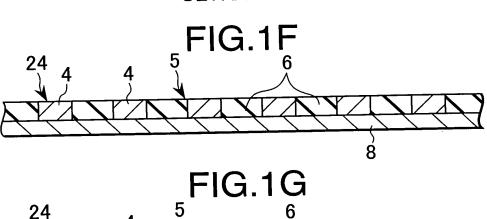


FIG.1D







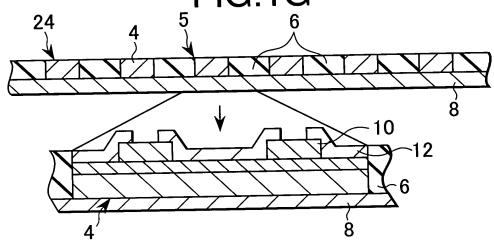


FIG.1H

13

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FIG.11

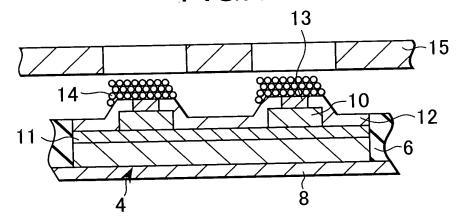


FIG.1J

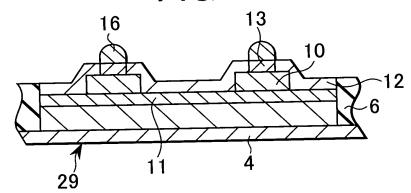


FIG.1K

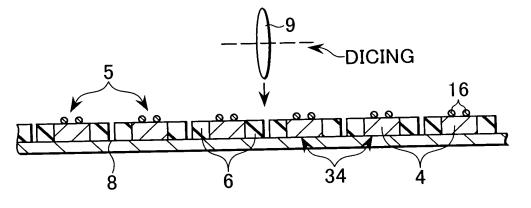


FIG.2

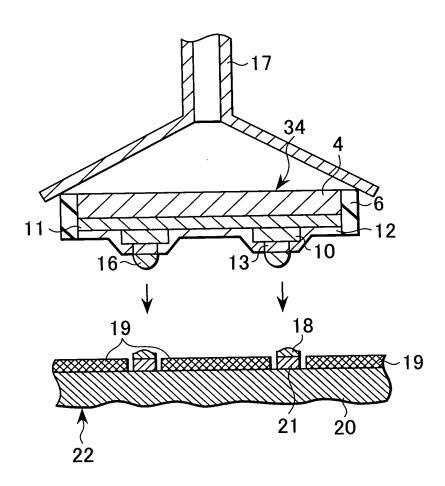


FIG.3

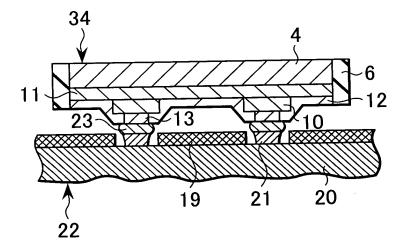
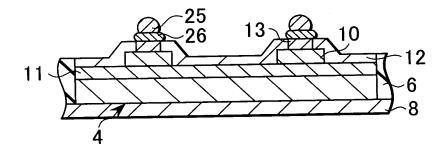


FIG.4





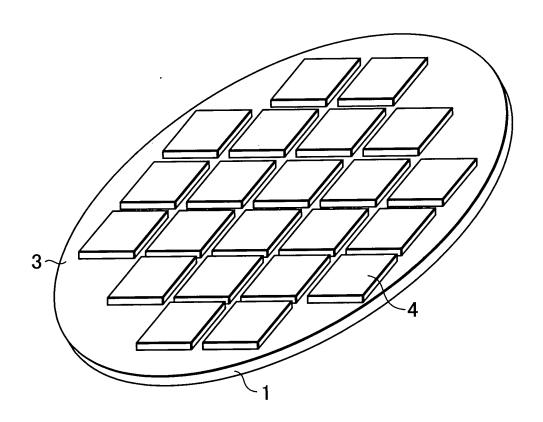
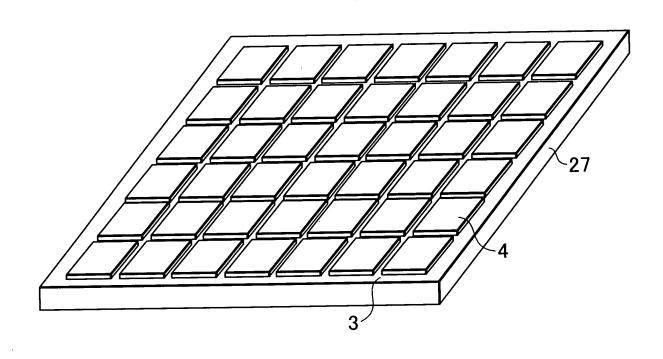
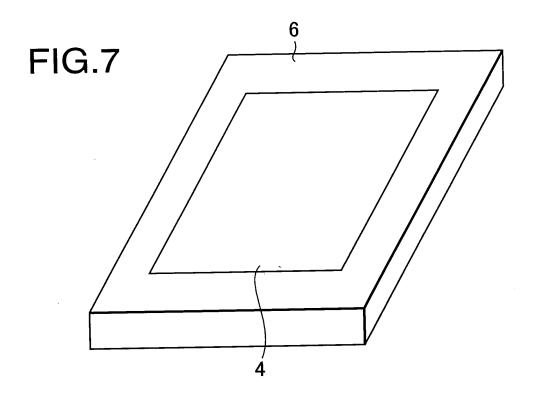


FIG.6





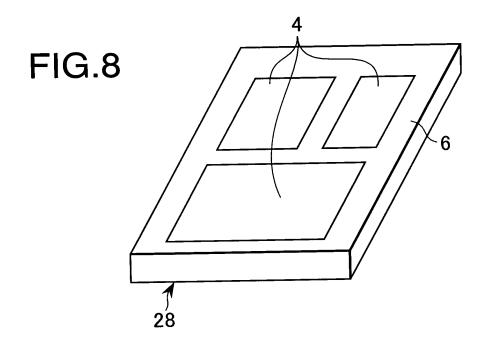
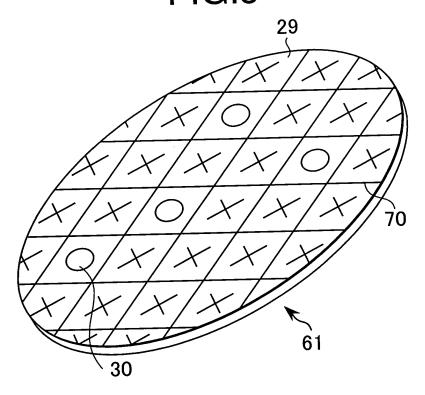


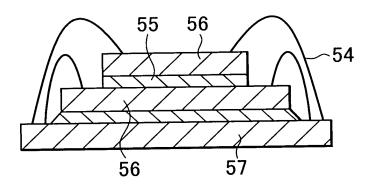
FIG.9

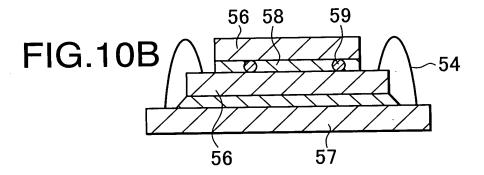


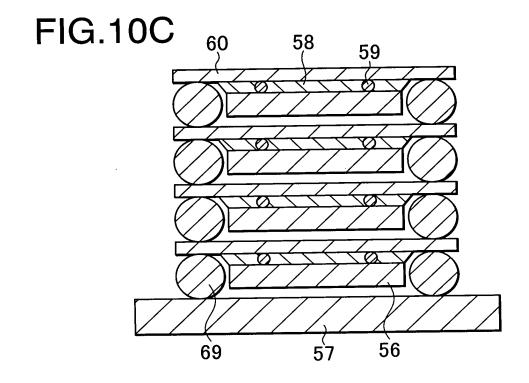
:NON-DEFECTIVE CHIP

X:DEFECTIVE CHIP

FIG.10A







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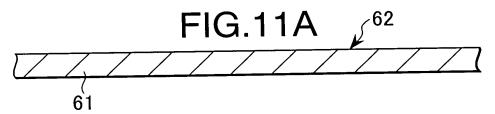


FIG.11B

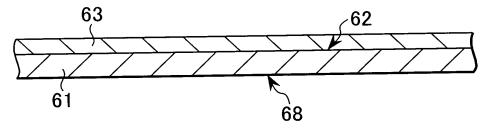


FIG.11C

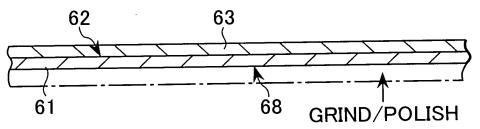


FIG.11D

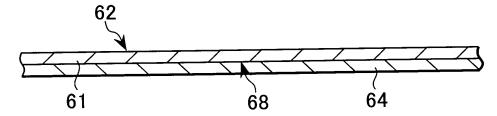
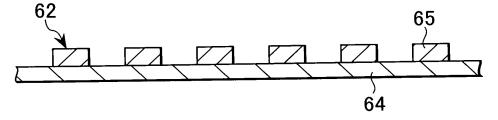
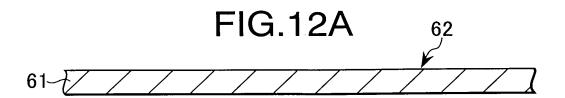
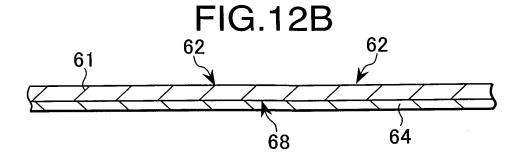


FIG.11E







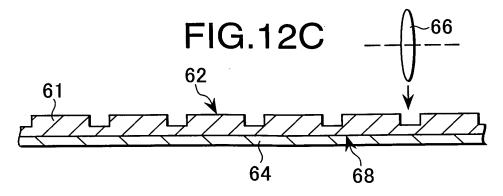


FIG.12D

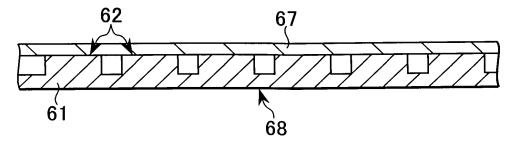


FIG.12E

